CLAIM AMENDMENT:

Please amend Claims 1, 4-6 and, 9-14 as follows:

Claim 1 (currently amended): A micro-controller controlling a data transfer to or from a host device through a pair of data lines for transferring a first data at the first data line and a second data at the second data line, which is different from the first data respectively, comprising:

an internal circuit;

a transfer control unit, which is operated in response to a oscillation signal, watching a condition of the data transfer at the pair of the data lines, and outputting a first output signal having a first logic level or a second logic level, and a third output signal having a first logic level or a second logic level as a watching result, the transfer control unit having a function for receiving the first data and the second data and transferring a desired data to the host device through the pair of data lines, wherein the third output signal is in the first logic level when the transfer control unit is in a condition of a ~~suspense~~ suspend mode, and the third output signal is in the second logic level when the transfer control unit is in a condition of a resume mode ;

a main control unit, which is operated by the oscillation signal, receiving the first output signal from the transfer control unit, and controlling an operation of the internal circuit in response to the first output signal having the second logic level, the main control unit changing its mode from an operative mode to an ~~inoperable~~ inoperative mode in response to the first output signal having the first logic level or from the inoperative mode to the ~~operable~~ operative mode in

response to the first output signal having the second logic level, and the main control unit outputting a second output signal having the first logic level when the main control unit is in the inoperative mode and outputting the second output signal having the second logic level when the main control unit is in the operative mode;

a logic circuit, which receives the second output signal and the third output signal, outputting fourth output signal, the fourth output signal being in the first logic level when both of the second and the third output signals have the first logic level, and the fourth output signal being in the second logic level when the logic levels of the second and the third output signals is in the other conditions; and

an oscillating circuit generating the oscillation signal having a frequency, the oscillating circuit being inactivated in response to the fourth output signal having the first logic level, and the oscillating circuit being activated in response to the fourth output signal having the second logic level, whereby the oscillating circuit is maintained to be in an operable ~~mode~~ state when one of the transfer control unit and the main control unit is in the operable ~~mode~~ state.

Claim 2 (original): A micro-controller, as claimed in claim 1, wherein the frequency of the oscillation signal is a first frequency, further comprising a clock signal generating circuit, which generates a clock signal having a second frequency that is higher than the first frequency by receiving the oscillation signal and sends the clock signal to the transfer control unit, the transfer control unit being operated by the clock signal.

Claim 3 (original;): A micro-controller, as claimed in claim 2 wherein the operation of the clock signal generating circuit is controlled in response to the watching result.

Claim 4 (currently amended): A micro-controller controlling a data transfer to or from a host device through a pair of data lines for transferring a first data at the first data line and a second data at the second data line, which is different from the first data respectively, comprising:

an internal circuit;

a transfer control unit, which is operated in response to a oscillation signal, watching a condition of the data transfer at the pair of the data lines, and outputting a first output signal as a watching result, the transfer control unit having a function for receiving the first data and the second data and transferring a desired data to the host device through the pair of data lines;

a main control unit, which is operated by the oscillation signal, receiving the first output signal from the transfer control unit, and controlling an operation of the internal circuit in response to the first output signal, the main control unit changing its mode from an operative mode to an ~~inoperable~~ inoperative mode or from the inoperative mode to the ~~operable~~ operative mode in response to the watching result, and the main control unit outputting a second signal when the main control unit is in the inoperative mode; and

an oscillating circuit generating the oscillation signal having a frequency, the oscillating circuit being inactivated in response to the second signal, and the

oscillating circuit being activated in response to the watching result when the main control unit returns to the ~~operable~~ operative mode;

wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to be in the ~~inoperable~~ inoperative mode when the transfer control unit detects the condition showing that the logic level of the first data is at the first level and the logic level of the second data is at the second level, which is different from the first level, for a particular period.

Claim 5 (currently amended): A micro-controller, as claimed in claim 4 wherein the transfer control unit sends the oscillating circuit the watching result for instructing the generation of the oscillation signal by detecting the condition showing that the logic level of the first data is at the second level and the logic level of the second data is at the first level while the main control unit is in the ~~inoperable~~ inoperative mode.

Claim 6 (currently amended): A micro-controller, as claimed in claim 5 wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to return to the ~~operable~~ operative mode when the transfer control unit detects the condition for a particular period showing that the logic levels of the first and second data are at the second level.

Claim 7 (previously presented): A micro-controller, as claimed in claim 5, further including a switch circuit selecting a first choice that a power supply

voltage of the main control circuit is supplied from the host device when the host is connected to the pair of the data lines, or selecting a second choice that a power supply voltage of the main control circuit is supplied from an external power supply voltage generating circuit when the host is connected to the pair of the data lines, the selection being made by a detection of the condition whether the host device is connected to the pair of the data lines, and the detection being made by a logic level of a voltage supplied from the host device.

Claim 8 (original): A micro-controller, as claimed in claim 7, further including an OR gate controlling to apply the watching result for instructing the generation of the oscillation signal to the oscillating circuit.

Claim 9 (currently amended): A micro-controller controlling a data transfer to or from a host device through a pair of data lines for transferring a first data at the first data line and a second data at the second data line, which is different from the first data respectively, comprising:

an internal circuit;

a transfer control unit, which is operated in response to a oscillation signal, watching a condition of the data transfer at the pair of the data lines, and outputting a first output signal as a watching result, the transfer control unit having a function for receiving the first data and the second data and transferring a desired data to the host device through the pair of data lines;

a main control unit, which is operated by the oscillation signal, receiving the first output signal from the transfer control unit, and controlling an operation of

the internal circuit in response to the first output signal, the main control unit changing its mode from an operative mode to an ~~inoperable~~ inoperative mode or from the inoperative mode to the ~~operable~~ operative mode in response to the watching result, and the main control unit outputting a second signal when the main control unit is in the inoperative mode; and

an oscillating circuit generating the oscillation signal having a frequency, the oscillating circuit being inactivated in response to the second signal, and the oscillating circuit being activated in response to the watching result when the main control unit returns to the ~~operable~~ operative mode;

wherein the frequency of the oscillation signal is a first frequency, further comprising a clock signal generating circuit, which generates a clock signal having a second frequency that is higher than the first frequency by receiving the oscillation signal and sends the clock signal to the transfer control unit, the transfer control unit being operated by the clock signal; and

wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to be in the ~~inoperable~~ inoperative mode when the transfer control unit detects the condition showing that the logic level of the first data is at the first level and the logic level of the second data is at the second level, which is different from the first level, for a particular period.

Claim 10 (currently amended): A micro-controller, as claimed in claim 9 wherein the transfer control unit sends the oscillating circuit the watching result for instructing the generation of the oscillation signal by detecting the condition

showing that the logic level of the first data is at the second level and the logic level of the second data is at the first level while the main control unit is in the ~~inoperable~~ inoperative mode.

Claim 11 (currently amended): A micro-controller, as claimed in claim 10 wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to return to the ~~operable~~ operative mode when transfer control unit detects the condition for a particular period showing that the logic levels of the first and second data are at the second level.

Claim 12 (currently amended): A micro-controller controlling a data transfer to or from a host device through a pair of data lines for transferring a first data at the first data line and a second data at the second data line, which is different from the first data respectively, comprising:

an internal circuit;

a transfer control unit, which is operated in response to a oscillation signal, watching a condition of the data transfer at the pair of the data lines, and outputting a first output signal as a watching result, the transfer control unit having a function for receiving the first data and the second data and transferring a desired data to the host device through the pair of data lines;

a main control unit, which is operated by the oscillation signal, receiving the first output signal from the transfer control unit, and controlling an operation of the internal circuit in response to the first output signal, the main control unit changing its mode from an operative mode to an ~~inoperable~~ inoperative mode or

from the inoperative mode to the ~~operable~~ operative mode in response to the watching result, and the main control unit outputting a second signal when the main control unit is in the inoperative mode; and

an oscillating circuit generating the oscillation signal having a frequency, the oscillating circuit being inactivated in response to the second signal, and the oscillating circuit being activated in response to the watching result when the main control unit returns to the ~~operable~~ operative mode;

wherein the frequency of the oscillation signal is a first frequency, further comprising a clock signal generating circuit, which generates a clock signal having a second frequency that is higher than the first frequency by receiving the oscillation signal and sends the clock signal to the transfer control unit, the transfer control unit being operated by the clock signal;

wherein the operation of the clock signal generating circuit is controlled in response to the watching result; and

wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to be in the ~~inoperable~~ inoperative mode when transfer control unit detects the condition showing that the logic level of the first data is at the first level and the logic level of the second data is at the second level, which is different from the first level, for a particular period.

Claim 13 (currently amended): A micro-controller, as claimed in claim 12 wherein the transfer control unit sends the oscillating circuit the watching result for instructing the generation of the oscillation signal by detecting the condition

showing that the logic level of the first data is at the second level and the logic level of the second data is at the first level while the main control unit is in the ~~inoperable~~ inoperative mode.

Claim 14 (currently amended): A micro-controller, as claimed in claim 13 wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to return to the ~~operable~~ operative mode when transfer control unit detects the condition for a particular period showing that the logic levels of the first and second data are at the second level.

Claim 15 (original): A micro-controller, as claimed in claim 1 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

Claim 16 (original): A micro-controller, as claimed in claim 2 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

Claim 17 (original): A micro-controller, as claimed in claim 3 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

Claim 18 (original): A micro-controller, as claimed in claim 4 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

Claim 19 (original): A micro-controller, as claimed in claim 5 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

Claim 20 (original): A micro-controller, as claimed in claim 6 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

Claim 21 (original): A micro-controller, as claimed in claim 7 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

Claim 22 (original): A micro-controller, as claimed in claim 8 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

Claim 23 (original): A micro-controller, as claimed in claim 10 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.